a loop filter coupled between the detector and the timing reference generator, the loop filter developing a control voltage for controlling the operational frequency of the timing reference generator,

wherein the timing reference signal generator is operatively configured to:

(a) produce an output signal at a characteristic frequency an integral multiple M of a desired output clock frequency, whereby the higher output frequency reduces, by the same integral multiple M, the number of output phases to be provided by the timing reference signal generator, and

(b) utilize the loop filter to facilitate the output of multi-phase signals, each phase signal oscillating at the characteristic frequency, whereby the number of phases represented by the multi-phase output signals are reduced by the integral multiple M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency;

a frequency divider circuit coupled to receive the output signal and reduce its characteristic frequency to a desired output clock frequency; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, the phase select MUX being a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

9. (Unchanged) The phase lock loop according to claim 8, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

10. (Unchanged) The phase lock loop according to claim 9, wherein the frequency divider circuit is constructed of current mode logic components.

11. (Unchanged) The phase lock loop according to claim 9, wherein the phase control MUX is constructed of current mode logic components.

21. (Twice Amended) A feedback controlled timing circuit, comprising:

a comparison circuit configured to compare a frequency characteristic of an input signal to a frequency characteristic of a timing reference signal, the comparison circuit asserting control signals in response to said comparison;

a timing reference signal generator, connected to provide a timing reference signal to the comparison circuit, the timing reference signal generator responsive, in feedback fashion, to said control signals asserted by the comparison circuit, the timing reference signal generator being configured to develop an output signal at a frequency an integral factor M times the frequency of a desired output clock signal, the desired output clock signal having a frequency characteristic an integral factor N times the frequency characteristic of the input signal, the timing reference signal generator being implemented as a VCO, the VCO constructed as a sequential delay stage and developing multi-phase output signals, each oscillating at the characteristic frequency of the VCO, and each having a phase relationship characterized by an inherent delay of each delay stage whereby the number of phases represented by the multi-phase output signals are reduced by the integral factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency;

first frequency divider circuitry disposed between the timing reference signal generator and the comparison circuit, the first frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor (NxM) to develop said frequency characteristic provided to said comparison circuit;

second frequency divider circuitry disposed between the timing reference signal generator and an output, wherein the first and second frequency divider circuitry having different frequency division characteristics, the second frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor M to develop said desired output clock signal; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, the phase select MUX being a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states